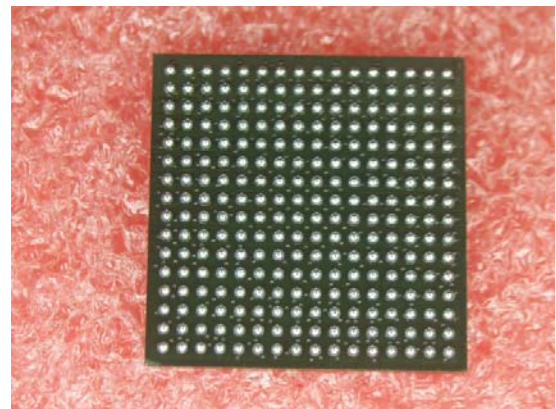




JTAG Electrical Test Report

Customer:		Order ref:	N/A
Manufacturer:	Altera Corporation	Requestor:	N/A
Part Number:	EP1C12F256C8N	Date/Time:	2015-09-11
Technician:	Roger Zuo	Received by:	Ouling
Datasheet:	http://www.altera.com.cn/literature/hb/cyc/cyc_c5v1.pdf		
Conclusion:	<p>Received 1,804 pieces and removed 1,728 for function testing on Application Board.</p> <p>Download program into device via Quartus and Download Cable, then observe if it is working correctly on Application Board.</p> <p>Found that 1,726 pieces passed testing with correct function and ID code, 2 pieces failed with program error.</p>		
Result:	Pass: 1,726 PCS; Fail: 2 PCS	Print Form	





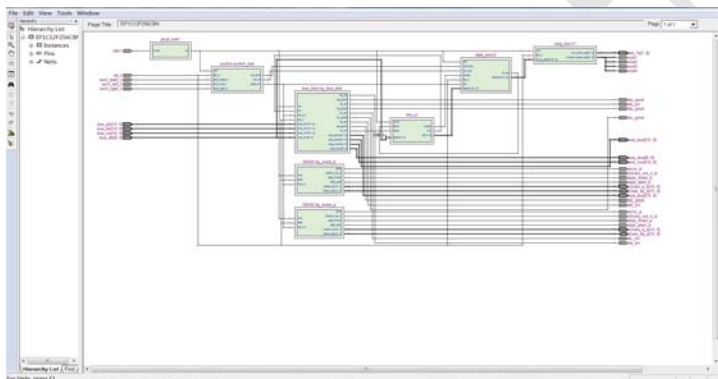
Component Information

Count QTY	1,804
Test QTY:	1,728
Package style	FBGA-256
Date code:	0845
Lot code:	Unknown
Kind of IC	IC FPGA 185 I/O 256FBGA

Test Results:

ID Error	No failed	If mixed, QTY:	
JTAG Error	failed	If mixed, QTY:	2
Function Error	No failed	If mixed, QTY:	
Expected function:	Passed	If mixed, QTY:	1,726
Equipment 1	Altera		
Equipment 2			

Test circuit Schematic



Description of Testing Procedure

Download program into device via Quartus and Download Cable, then observe if it is working correctly.

Test Program

```

21 module EP1C12F256C8N(
22     clk1n1, rst_n,
23     sw3_left_n, sw4_right_n, sw2_start_n,
24     led_7s, wei1, wei2, wei3, wei4,
25
26     oSram_a_a, sram_dq_a, oSram_we_n_a, error_a, task_start_a, task_finish_a,
27     oSram_a_b, sram_dq_b, oSram_we_n_b, error_b, task_start_b, task_finish_b,
28
29     bus_ain, bus_aout,
30     bus_bin, bus_bout,
31     bus_cin, bus_cout,
32     bus_din, bus_dout,
33     ba_err, bb_err, bc_err, bd_err,
34     ba_good, bb_good, bc_good, bd_good
35 );
36
37 input clk1n1; //50MHz
38
39 input rst_n;
40
41 input sw3_left_n;
42 input sw4_right_n;
43 input sw2_start_n;
44
45 output [7:0] led_7s;
46 output wei1;
47 output wei2;
48 output wei3;
    
```

Messages:

- Info: Changed top-level design entity name to "EP1C12F256C8N"
- Info: Started Full Compilation at Wed Sep 02 16:31:46 2015 中国标准时间
- Info: Ended Full Compilation at Wed Sep 02 16:31:52 2015 中国标准时间
- Info: Successfully loaded and ran Tcl Script File "E:\project\FPGA\Altera\EP1C12F256C8N\EP1C12F256C8N_new\EP1C12F256C8N.tcl"
- Info: Started Full Compilation at Wed Sep 02 16:32:03 2015 中国标准时间
- Info: Ended Full Compilation at Wed Sep 02 16:32:25 2015 中国标准时间

IC Pin Assignment

Top View - Wire Bond
Cyclone - EP1C12F256C8N

Node Name	Direction	Location	I/O Bank	VREF Group	Reserved	Group	PCB layer	I/O Standard	Current Strength
Sram_dq_a[15..0]	Bidir	PNL_C2	1	B1_N0		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[14]	bidir	PNL_D1	1	B1_N0		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[13]	bidir	PNL_D2	1	B1_N0		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[12]	bidir	PNL_E1	1	B1_N0		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[11]	bidir	PNL_M4	1	B1_N2		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[10]	bidir	PNL_M3	1	B1_N2		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[9]	bidir	PNL_M4	1	B1_N2		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[8]	bidir	PNL_F3	1	B1_N2		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[7]	bidir	PNL_N1	1	B1_N2		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[6]	bidir	PNL_M2	1	B1_N2		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[5]	bidir	PNL_M1	1	B1_N2		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[4]	bidir	PNL_M2	1	B1_N2		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[3]	bidir	PNL_L1	1	B1_N2		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[2]	bidir	PNL_L2	1	B1_N2		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[1]	bidir	PNL_K1	1	B1_N2		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)
Sram_dq_a[0]	bidir	PNL_K2	1	B1_N1		Sram_dq_a[15..0]		3.3-V LVTTTL (def...)	24mA (default)

